DATA SHEET

ADDENDUM

SL2 ICS 20

I²CODE SLI Label IC

Bumped Wafer Specification

Product Specification

Revision 3.0

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PHILIPS

Bumped Wafer Specification SL2 ICS 20

CONTENTS

Bumped Wafer Specification SL2 ICS 20

1 SCOPE

This specification describes the electrical, physical and dimensional properties of Au-bumped sawn wafers on FFC of I•CODE[1] SLI Label ICs on a Philips C075EE process and is the base for delivery of tested I•CODE SLI Label ICs.

2 REFERENCE DOCUMENTS

2.1 Philips Documents

- MIL-STD 883D Method 3023
- MIL-STD 883D Method 3015
- SNW-FQ-627
- PICTOH-QS007
- General Specification for 8" Wafer
- General Quality Specification
- I•CODE SLI Label IC, Functional Specification
- Application Note Coil Design Guide
- Specification of the IBIS Wafermap

3 MECHANICAL SPECIFICATION

3.1 Wafer

- Diameter: 8"
- Thickness: 150 µm ± 15 µm
- Flatness: max. tbf

3.2 Wafer Backside

- Material: Si
- Treatment: ground + stress releave
- Roughness: R_a max. 0.5 µm
  R_t max. 5 µm

3.3 Chip Dimensions

- Chip size: 900 x 780 µm
- Scribe lines: 80 / 80 µm

3.4 Passivation

- Type: sandwich structure
- Material: PSG / Nitride (on top)
- Thickness: 500 nm / 600 nm

3.5 Au Bump

- Bump material: > 99.9% pure Au
- Bump hardness: 35 – 80 HV 0.005
- Bump shear strength: > 70 MPa
- Bump height: 18 µm
- Bump height uniformity:
  - within a die: ± 2 µm
  - within a wafer: ± 3 µm
  - wafer to wafer: ± 4 µm
- Bump flatness: ± 1.5 µm
- Bump size:
  - LA, LB 92 x 92 µm
  - VSS[2], TESTIO 62 x 62 µm
- Pad size (no bump!)
  - LA, LB 78 x 78 µm
  - VSS[3], TESTIO 48 x 48 µm
- Bump size variation: ± 5 µm
- Under bump metallisation: sputtered TiW

4 FAIL-DIE IDENTIFICATION

Every die is electrically tested according to data sheet. Identification of chips with electrical parameters not conform with the data sheet is done by inking and wafer mapping (all dies at wafer periphery are identified as 'FAIL').

The ink information refers to unsawn wafers. At sawn wafers (on FFC) additional ICs are be marked as 'FAIL' in the wafer map if damaged during the sawing process. These ICs will not be inked.

4.1 Wafer Mapping

Wafer mapping for failed die information is available on Floppy-Disk.

Format: IBIS format

5 ORDERING INFORMATION

5.1 Bumped die on sawn wafer

- Order Code: SL2 ICS20 01DW/V4D
- 12NC: 9352 716 15005

[1] I•CODE is a registered trademark of Philips Electronics N.V.

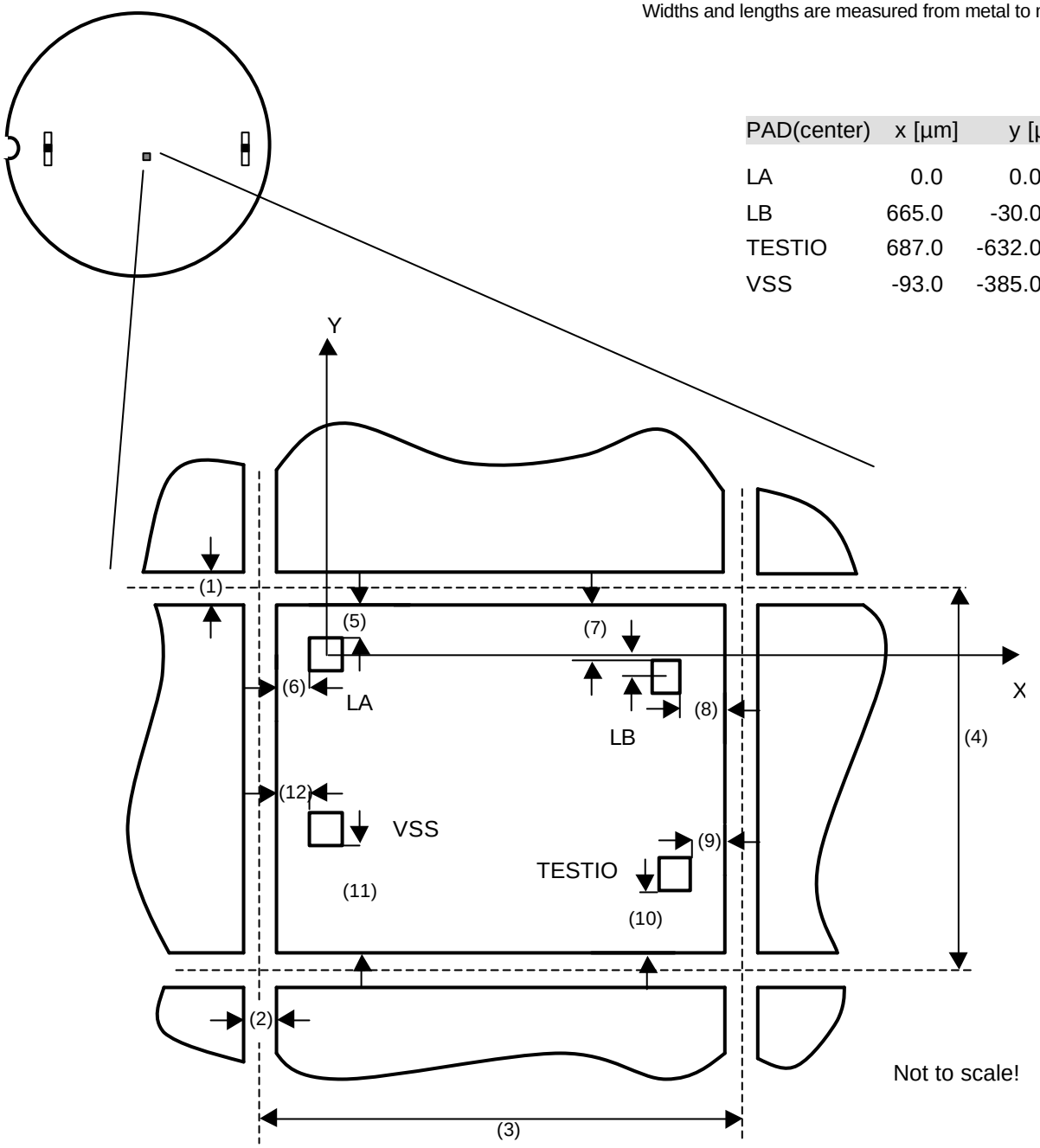
[2] VSS is conntected to substrate.

[3] VSS is conntected to substrate.

6 CHIP ORIENTATION AND BONDPAD LOCATIONS

Widths and lengths are measured from metal to metal.

PAD(center)	x [µm]	y [µm]
LA	0.0	0.0
LB	665.0	-30.0
TESTIO	687.0	-632.0
VSS	-93.0	-385.0



(1) X-Scribeline width: tbd µm
(2) Y-Scribeline width: tbd µm
(3) Chip step, x-length: X-Scribeline + 900 µm
(4) Chip step, y-length: Y-Scribeline + 780 µm
(5) LA bump edge to chip edge, y-length: 39[+7] µm
(6) LA bump edge to chip edge, x-length: 104[+7] µm
(7) LB bump edge to chip edge, y-length: 69[+7] µm
(8) LB bump edge to chip edge, x-length: 39[+7] µm
(9) TESTIO bump edge to chip edge, x-length: 32[+7] µm
(10) TESTIO bump edge to chip edge, y-length: 32[+7] µm
(11) VSS bump edge to chip edge, y-length: 279[+7] µm
(12) VSS bump edge to chip edge, x-length: 26[+7] µm

[+7µm] ...*for pad edge to chip edge!*

Figure 1

7 ELECTRICAL SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
T_{stg}	Storage Temperature Range		- 55 to +140	°C
T_j	Junction Temperature		- 55 to +140	°C
V_{ESD}	ESD Voltage Immunity	MIL-STD-883D, Method 3015.7, Human Body Model	± 2	kV_{peak}
$I_{max\ LA-LB}$	Maximum Input Peak Current		± 60	mA_{peak}

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

7.2 OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$T_{j\ op}$	Operating Junction Temperature		- 25		+ 85	°C
I_{LA-LB}	Input Current[2]				30	mA_{rms}
V_{LA-LB}	Minimum Supply Voltage for READ/WRITE/EAS		± 2.5	± 2.6	± 2.9	V_{rms}
f_{op}	Operating Frequency[3]		13.553	13.560	13.567	MHz

NOTES:

1. Typical ratings are not guaranteed. These values listed are at room temperature.

2. The voltage between LA and LB is limited by the on-chip voltage limitation circuitry (corresponding to parameter I_{LA-LB}).

3. Bandwidth limitation (±7 kHz) according to ISM band regulations.

7.3 ELECTRICAL CHARACTERISTICS

T_{jop} = - 25 to +85 °C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
C_{res}	Input Capacitance between LA - LB[2]	$V_{LA-LB} = 2\ V_{rms}$	22.3	23.5	24.7	pF
P_{min}	Minimum Operating Supply Power[3]			280		µW
m	Modulation of RF Voltage for Demodulator Response	$m = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}$	**	**	**	%
$t_{P\ sm}$	Modulation Pulse Length of RF Voltage		**	**	**	µs
t_D	Demodulator Response Time	m ≥ 10 %, 100%	**	**	**	µs
R_{mod}	Load Modulation		**	**	**	Ω
t_{ret}	EEPROM Data Retention	$T_{amb} \leq 55$ °C	10			Years
n_{write}	EEPROM Write Endurance		100 000			Cycles

NOTES:

1. Typical ratings are not guaranteed. These values listed are at room temperature.

2. Measured with an HP4285A LCR meter at 13.56 MHz.

3. Including losses in resonant capacitor and rectifier.

** : refer to ISO/IEC 15693-2 and 15693-3 including pulse shapes and tolerances; proper coil design assumed

8 FINAL WAFERTEST SPECIFICATION

- Minimum yield per wafer: 30% of 35416 potential good dies .
- Minimum yield per lot: 30%

9 HINTS FOR LABEL IC ENCAPSULATION

9.1 Protection against Visible Light

As a result of the ultra low power design of the I•CODE SLI Label IC some analogue circuits on the chip are light sensitive. This means that common sun light can impact the operation of the label if the chip is not protected against visible light radiation.

Measurements have shown that a radiation of E_{max} = 60 W/m^2 (spectrum: 400 to 1000 nm) causes a reduced operating range of the plain chip.

Measurements of direct sunlight in summer deliver values up to 260 W/m^2.

To ensure proper operation an expected minimum radiation reduction factor of approx. 9 (2 x 260/60 = 8.7) must be provided by the encapsulation. That means special care has to be taken to ensure a sufficient light protection of the I•CODE SLI Label IC (e.g. non translucent encapsulation or underfiller, ...) according to application requirements.

9.2 Protection against UV Light

An EEPROM memory, as it is also used in the I•CODE SLI Label IC, has some principle sensitivity to UV light (applies to EEPROM-technology in general).

Thus strong UV exposure in the production of inlets/labels has to be avoided. UV protection has to be ensured using appropriate assembly methods.

9.3 Resistance to X-Rays

X-ray exposure on comparable Philips ICs (with even smaller feature size) caused neither a long term influence on the behaviour of the ICs nor on the data retention of the EEPROMs.

10 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics section of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

11 DISCLAIMERS

11.1 Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so on their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

11.2 Licence Policy

Purchase of this Philips IC with a functionally according to ISO/IEC 15693 Standard does not convey an implied license under any patent right on this standard. A license for the Philips portfolio of patents on the ISO/IEC 15693 Standard can be obtained via the Philips Intellectual Property and Standards department. For more information please contact the nearest Philips Semiconductors sales office.

12 REVISION HISTORY

Table 1 Bumped Wafer Specification SL2 ICS20 Revision History

REVISION	DATE	CPCN	PAGE	DESCRIPTION
1.0	Sept. 2000	-		Initital version.
1.1	Feb. 2002			New die size and dimensions
2.0	June 2002			Preliminary Specification
2.1	Sept. 2002		3	Include IBIS Wafermap
3.0	Dec. 2002			Product Specification

NOTES

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